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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	<b>Application Number</b>	10/020,388
	<b>Filing Date</b>	December 14, 2001
	<b>First Named Inventor</b>	William Salkewicz
	<b>Group Art Unit</b>	2152
	<b>Examiner Name</b>	Not yet assigned
<b>Total Number of Pages in This Submission</b>		<b>Attorney Docket Number</b> 4906.P001D

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Sheet 1 of 4

## **Complete if Known**

Application Number	10/020,388
Filing Date	December 14, 2001
First Named Inventor	William Salkewicz
Art Unit	2152
Examiner Name	Not yet assigned
Attorney Docket Number	4906.P001D

## **U.S. PATENT DOCUMENTS**

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
		US- 5659796	08-19-1997	Thorson et al.	
		US- 5604680	02-18-1997	Bamji et al.	
		US- 5684974	11-04-1997	Onodera	
		US- 5692193	11-25-1997	Jagannathan et al.	
		US- 5761477	06-02-1998	Wahbe et al.	
		US- 5784707	07-21-1998	Khalidi et al.	
		US- 6105027	08-15-2000	Schneider et al.	
		US- 6128665	10-03-2000	Iturralde	
		US- 6219699 - B1	04-17-2001	McCloghrie et al.	
		US- 6223218 - B1	04-24-2001	Iijima et al.	
		US- 6226751	05-01-2001	Arrow et al.	
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## **FOREIGN PATENT DOCUMENTS**

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Sheet 2 of 4

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Filing Date	December 14, 2001
First Named Inventor	William Salkewicz
Group Art Unit	2152
Examiner Name	Not yet assigned
Attorney Docket Number	4906.P001D

**OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS**

Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s) publisher city and/or country where published	T <sup>2</sup>
		Adve, V., et al., "Performance Analysis of Mesh Interconnection Networks with Deterministic Routing," IEEE Transactions on Parallel and Distributed Systems, Vol. 5, No. 3, pp. 225-246, March 1994.	
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		Comer, D., "Computer Networks and Internets," Prentiss Hall, 1997.	
		Cmelik, B., et al., "Shade: A Fast Instruction - Set Simulator for Execution Profiling," ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems, pp. 128-137, May 1994.	
		Dally, W.J., et al., "Deadlock-Free Message Routing in Multiprocessor Interconnection Networks," IEEE Transactions on Computers, Vol. C-36, No. 5, pp. 547-553, May 1987.	
		Dally, W.J., "Virtual-Channel Flow Control," Proc. 17th International Symposium on Computer Architecture, pp. 60-68, May 1990.	
		Dally, W.J., "Performance Analysis of k-ary n-cube Interconnection Networks," IEEE Transactions on Computers, Vol. 39, No. 6, pp. 775-785, June 1990.	

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Sheet 3 of 4

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		Dally, W.J., et al., "Deadlock-Free Adaptive Routing in Multicomputer Networks Using Virtual Channels," IEEE Transactions on Parallel and Distributed Systems, Vol. 4, No. 4, pp. 466-475, April 1993.	
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Sheet 4 of 4

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		Leinwand, A., et al., Cisco Router Configuration, MacMillan Technical Publishing, Indianapolis, IN, 1998.	
		Li, K., et al., "Memory Coherence in Shared Virtual Memory Systems," ACM Transactions on Computer Systems, Vol. 7, No. 4, pp. 321-359, November 1989.	
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		Luckham, D., et al., "Verification of Array, Record, and Pointer Operations in Pascal," ACM Transactions on Programming Languages and Systems, Vol. 2, No. 2, pp. 226-244, October 1979.	
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